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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,328	12/20/2001	Wen-Jie Qi	50432-485	2309

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EXAMINER
VINH, LAN

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 04/03/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,328	QI ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement (IDS) filed on 3/21/2002 has been considered. The PTO form 1449 is enclosed with this office action.

Drawings

2. The drawing 6a is objected to because of the following minor informalities: on the left side of gate electrode 22, part 32 should be labeled as 34 and part 34 should be labeled as 32 to be consistent with the right side of the gate electrode. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4, 6, 7, 8, 9, 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Ramaswami (US 5,783,475)

Ramaswami discloses a method of forming a spacer. This method comprises the steps of:

forming a gate electrode (polysilicon) 32 on a substrate 31 (col 2, lines 17-18)

forming a dielectric layer 48 by thermal reoxidation of the gate electrode 32 (polysilicon), the layer 48 is formed over the substrate 31 and gate electrode 32 (col 2, lines 1-3, lines 40-42, fig. 2), which reads on forming a polysilicon reoxidation layer over the substrate and the gate electrode since the polysilicon reoxidation layer is defined as a dielectric layer on page 5 of the specification.

forming a nitride layer 36 over layer 48/polysilicon reoxidation layer (col 3, lines 1-2)

using an anisotropic etchant to etch the nitride layer 36 to remove layer 36 (as shown in fig. 5) to form spacers 36 on the portions of layer 48 on the sidewall of the gate electrode 32, the etching stop on layer 48 (col 4, lines 32-33), which reads on anisotropically etching the nitride layer and stopping on the polysilicon reoxidation layer to form nitride offset spacers on the gate electrode since the offset spacer is defined as a nitride portion and a polysilicon reoxidation portion on the sidewall of the gate electrode on page 6 of the specification.

Regarding claim 2, Ramaswami discloses forming doped source regions 34 and doped drain region 35 extending from source region 43 and drain region 44 (fig. 5), which reads on forming source/drain extension in the substrate after the nitride layer 36 has been etched, forming spacers 37 on the offset spacer (36 and 41) (col 4, lines 50-55,

Regarding claim 4, Ramaswam discloses performing a reactive ion etch (RIE) with selectivity between the oxide and nitride layer (col 3, lines 40-46)

Regarding claim 6, Ramaswami discloses that the dielectric layer 48/ polysilicon reoxidation layer is about 50-200 angstroms thick (col 2, lines 41-42) overlaps the claimed range of 15-50 angstroms.

Regarding claim 7, Ramaswami discloses performing the RIE uses a plasma containing CHF_3 gas (col 3, lines 40-42)

Regarding claim 8, fig. 6 of Ramaswami shows that the exposed dielectric layer 48/ polysilicon reoxidation layer is removed after nitride layer 36 has been etched .

Regarding claims 9, 10, Ramaswami discloses the step of dielectric removal using wet etch comprised of HF acid which has a selectivity of greater than 100:1 (col 5, lines 3-6), which reads on wet etching the exposed polysilicon reoxidation layer with 100:1 HF solution.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3,11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramaswami (US 5,783, 475) in view of Hong (US 5,899,719)

Ramaswami discloses a method of forming a spacer. This method comprises the steps of:

forming a gate electrode (polysilicon) 32 on a subtrate 31 (col 2, lines 17-18)

forming a dielectric layer 48 on the substrate 31 (col 2, lines 39-41), fig. 5 of Ramaswami shows that the step of etching layer 36 stops on layer 48, which reads on forming an etch stop layer on the substrate

forming a nitride layer 36 on the layer 48/etch stop layer (col 3, lines 1-2, fig. 3)

using an anisotropic etchant to etch the nitride layer 36 to remove layer 36 to form spacers 36 on the portion of layer 48 on the sidewall of the gate electrode 32, the etching stop on layer 48 (col 4, lines 32-33, fig. 5), which reads on etching the nitride layer and stopping the etching on the etch stop layer to form nitride offset spacers on the gate electrode since the offset spacer is defined as a nitride portion and a polysilicon reoxidation/etch stop portion on the sidewall of the gate electrode on page 6 of the specification.

Unlike the instant claimed inventions as per claims 3, 11, Ramaswami fails to disclose the step of forming halo implants in the substrate prior to depositing the nitride layer.

However, Hong discloses a method for forming a narrow gate FET (Field effect transistor)/semiconductor device comprises the step of forming a pocket or halo implantation adjacent to the gate electrode and opposite to that of the source/drain region in the substrate after the gate electrode is defined (col 4, lines 40-48). Hong's teaching reads on the step of forming halo implants in the substrate prior to depositing the nitride layer.

Hence, one skilled in the art would have found it obvious to modify Ramaswamin' s method by adding the step of forming halo implants in the substrate as per Hong

because Hong teaches that the forming of the halo implant reduces the size of the P/N junction that is formed between the source/drain region and reducing the size of this P/N junction can increase the operating speed of the FET/semiconductor device (col 4, lines 48-52)

Regarding claim 12, Ramaswami discloses forming a dielectric layer 48 by thermal reoxidation of the gate electrode 32 (polysilicon) (col 2, lines 1-3, lines 40-42), which reads on forming a polysilicon reoxidation layer 48/etch stop layer

Regarding claim 13, Ramaswami discloses forming doped source regions 34 and doped drain region 35 extending from source region 43 and drain region 44 by implantation after etching the nitride layer to form the spacer (fig. 1, fig. 5),

Regarding claim 14, fig. 6 of Ramaswami shows that the dielectric layer 48/polysilicon reoxidation layer is removed exposing the substrate.

Regarding claim 15, Ramaswami discloses the step of dielectric removal using wet etch comprised of HF acid (col 5, lines 3-6), which reads on wet etching the polysilicon reoxidation layer

Regarding claims 16, 17, Ramaswam discloses performing a reactive ion etch (RIE) with selectivity between the oxide and nitride layer (col 3, lines 40-46), fig. 5 of Ramaswami shows that nitride layer 36 is being removed faster than dielectric (oxide) layer 48 after the RIE etching, which reads on etching the nitride layer with a plasma etchant that has high nitride to oxide selectivity.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramaswami (US 5,783, 475) in view of Tseng et al (US 6,063,698)

Ramaswami's method has been described above in paragraph 4. Unlike the instant claimed invention as per claim 5, Ramaswami does not specifically disclose forming the polysilicon reoxidation layer by thermally growing oxide on the substrate and the gate electrode at a temperature between about 700-900^0 C.

Tseng discloses a method of manufacturing a semiconductor device comprises the step of thermally growing oxide on the substrate and the gate electrode 20 at a temperature lower than 750-850^0 C. (col 6, lines 22-26)

Hence, one skilled in the art would have found it obvious to modify Ramaswamin' step of forming the polysilicon reoxidation layer by thermally growing oxide on the substrate and the gate electrode at a temperature range as taught by Tseng because Tseng states that the lower temperature (750-850^0 C) environment ensures that the thickness of the dielectric over the gate electrode is relatively thin, whereby consumption of the polysilicon electrode is minimized (col 6, lines 28-31)

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

LV
April 2, 2003